

EXHIBIT F

U.S. Patent No. 6,724,241 (“’241 Patent”)

Accused Products

LG products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the LG V50 ThinQ (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent.

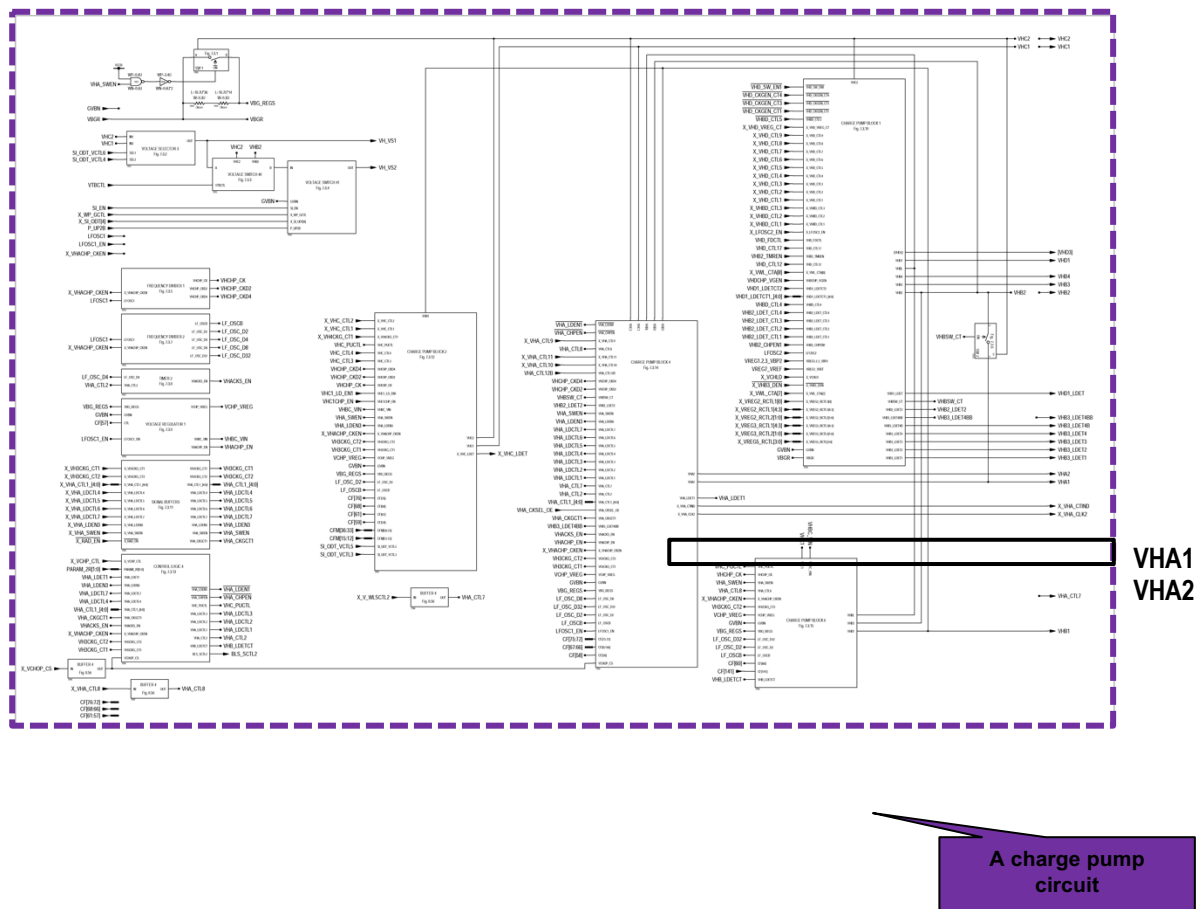
Claim 1

Claim 1	Accused Product
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the V50 ThinQ includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

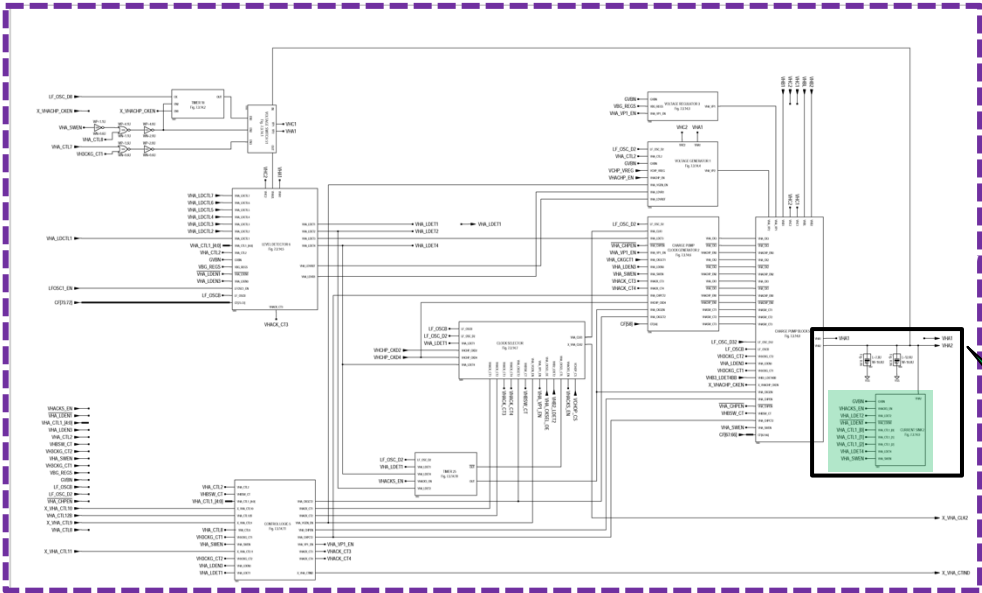
Claim 1	Accused Product
	<div> <div> <div> 3 - SanDisk #SDINDDH4-128G Multichip Memory - 128 GB 3D TLC NAND Flash, Memory Controller (UFS 2.1) (5-Die Pkg.) Pkg Size: 13 x 11.51 mm </div> <div> 3.1 - SanDisk #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.16 x 6.26 mm </div> <div> 3.2 - SanDisk #EAGLEMP28 Memory Controller (UFS 2.1) Die Size: 5.02 x 2.27 mm </div> <div> <p><u>Function:</u></p> <div>Memory: Non-Volatile</div> </div> </div> <div> <p>The micrograph shows a large integrated circuit package. A red box labeled '4x Die' points to the top section of the package. A red box labeled '3.2 - SanDisk #EAGLEMP28 Memory Controller (UFS 2.1) Die Size: 5.02 x 2.27 mm' points to a small die located at the bottom right of the package. A red box labeled '3.1 - SanDisk #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.16 x 6.26 mm' points to a large die located in the center of the package.</p> </div> </div>

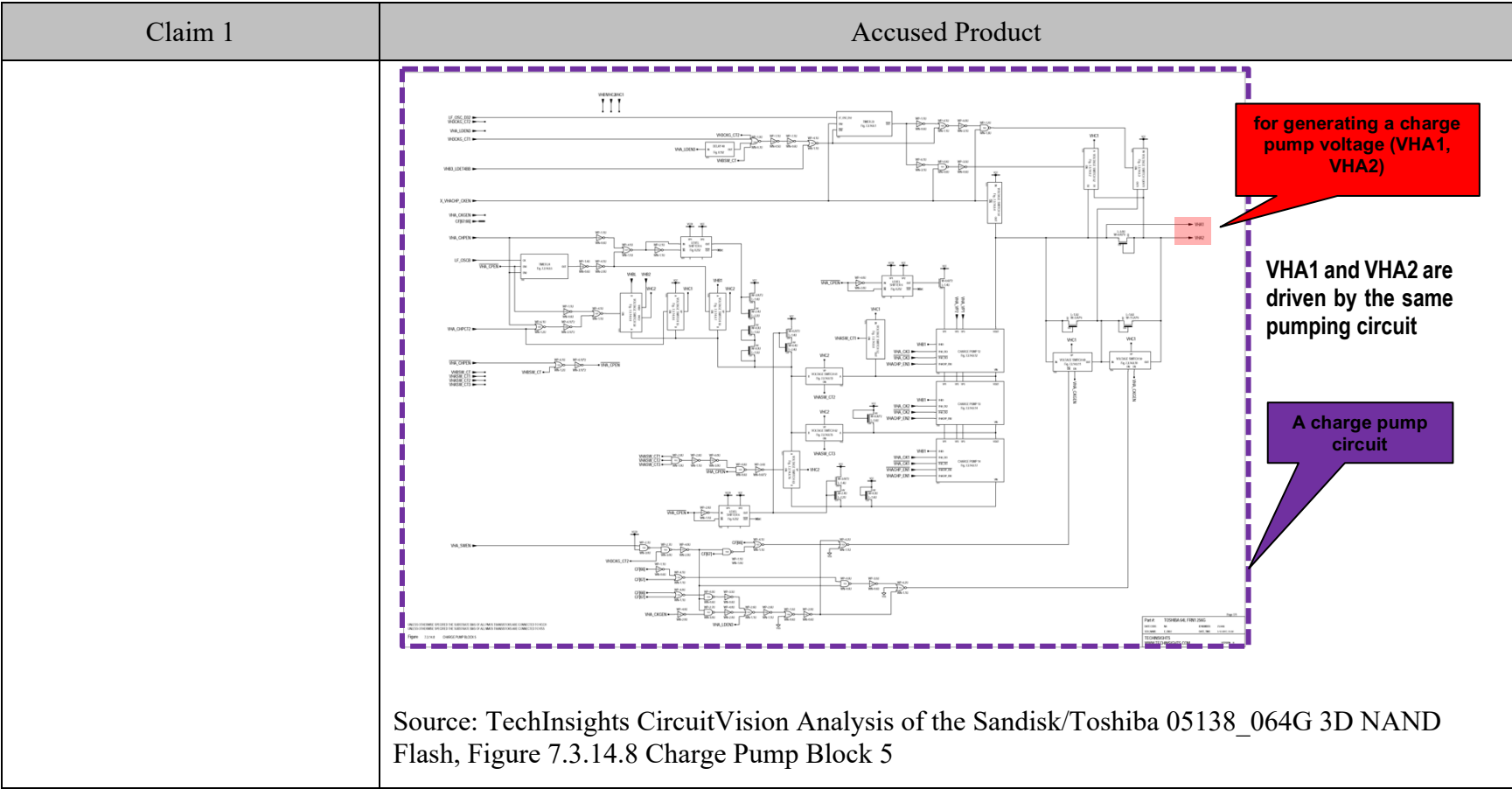
Claim 1

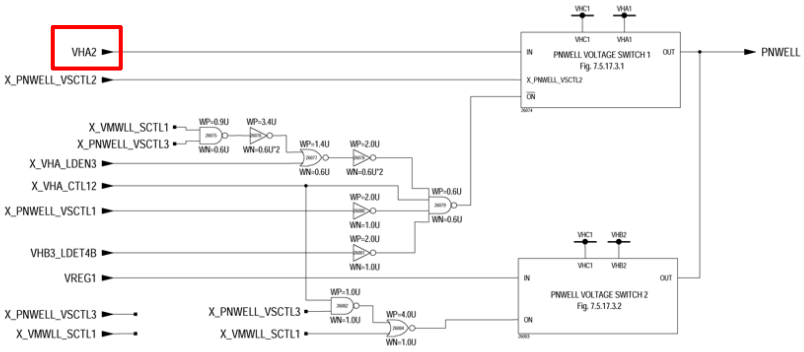
Accused Product

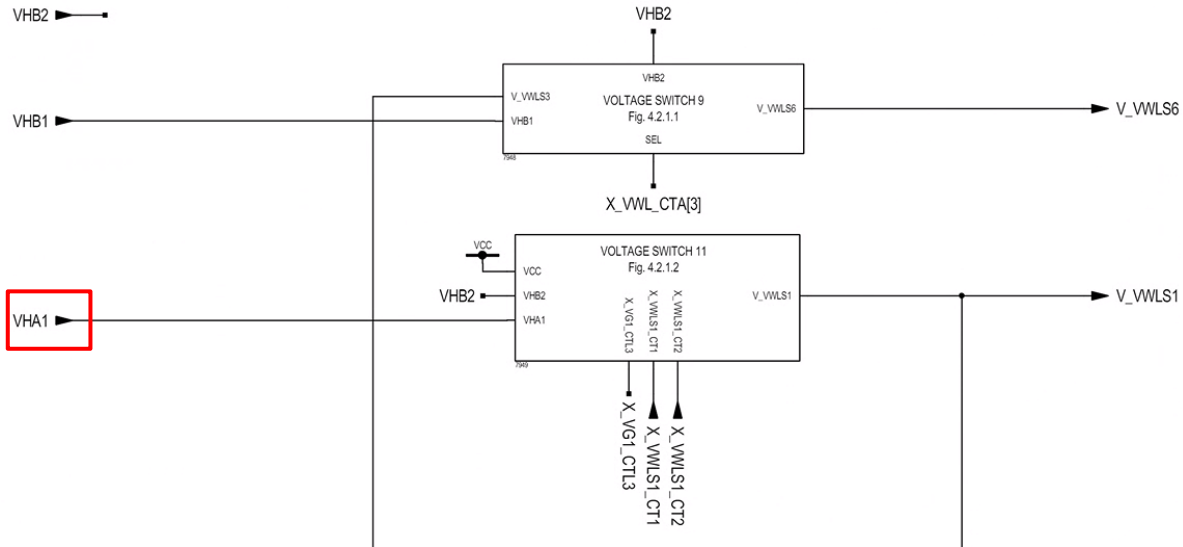


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

Claim 1	Accused Product
	<div data-bbox="630 264 1606 852"></div> <p data-bbox="630 933 1827 1015">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System</p>



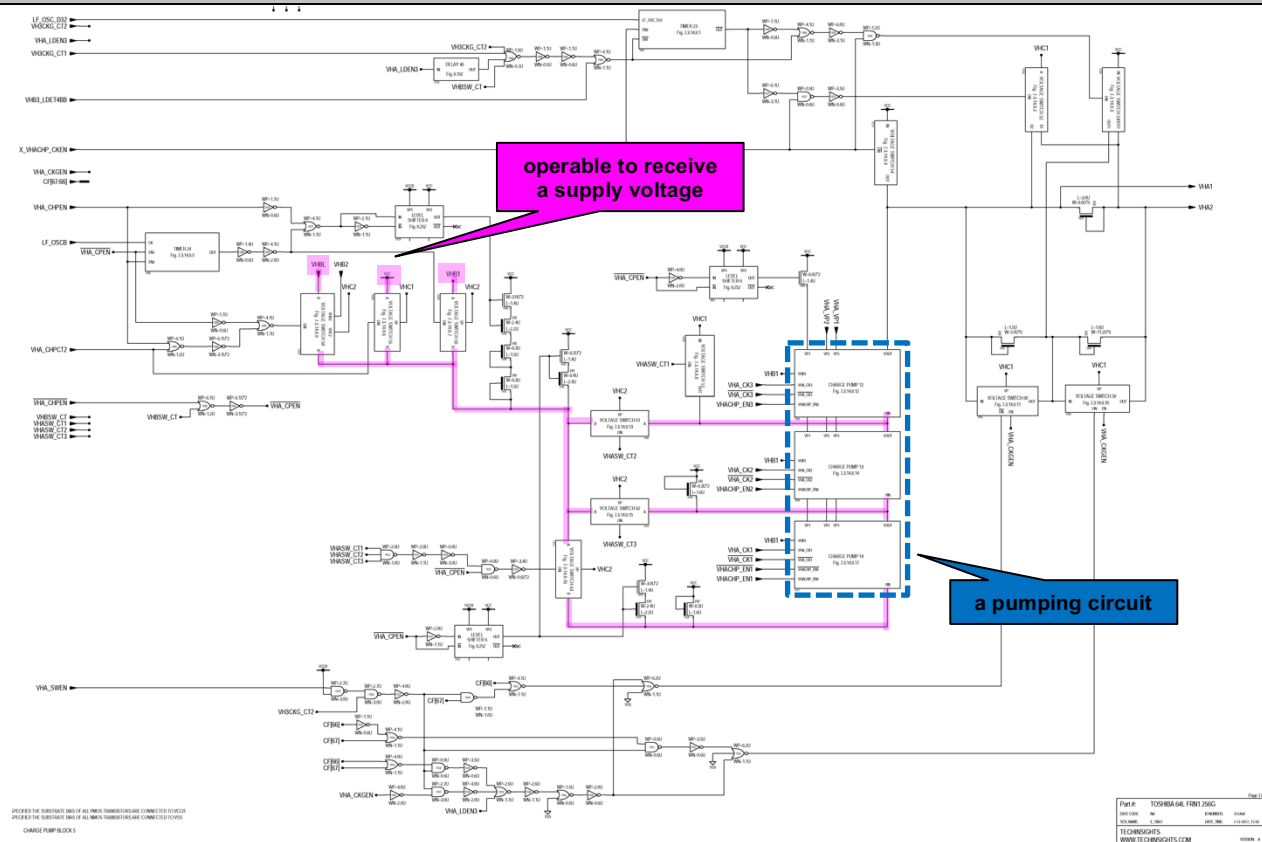
Claim 1	Accused Product
	<p data-bbox="688 267 1255 332">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>  <p data-bbox="634 771 1831 844">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Product
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out</p>

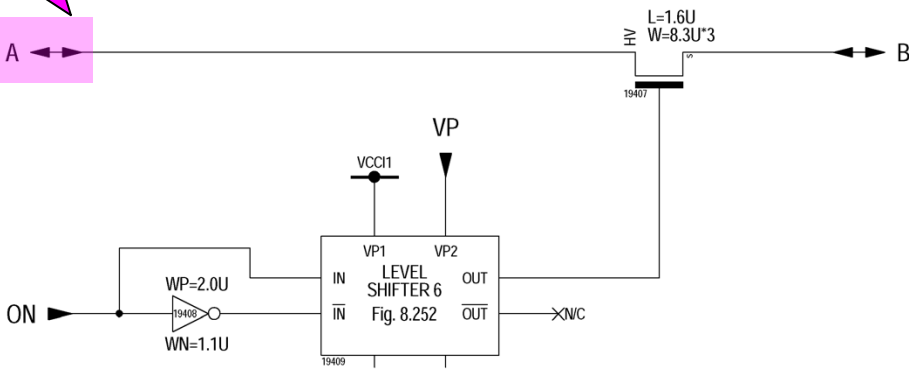
Claim 1	Accused Product
	<p>resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

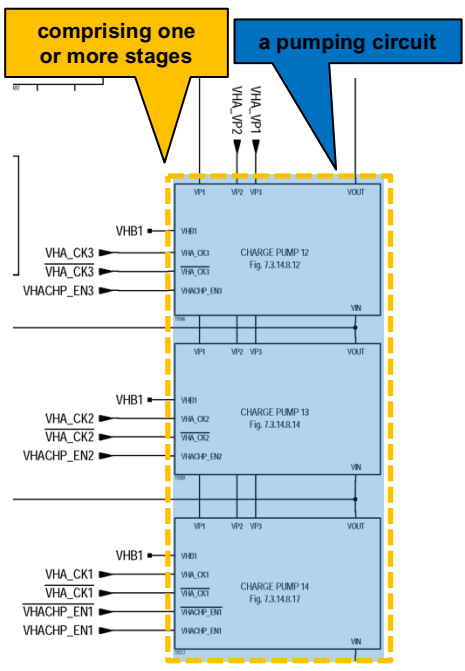
Claim 1

Accused Product



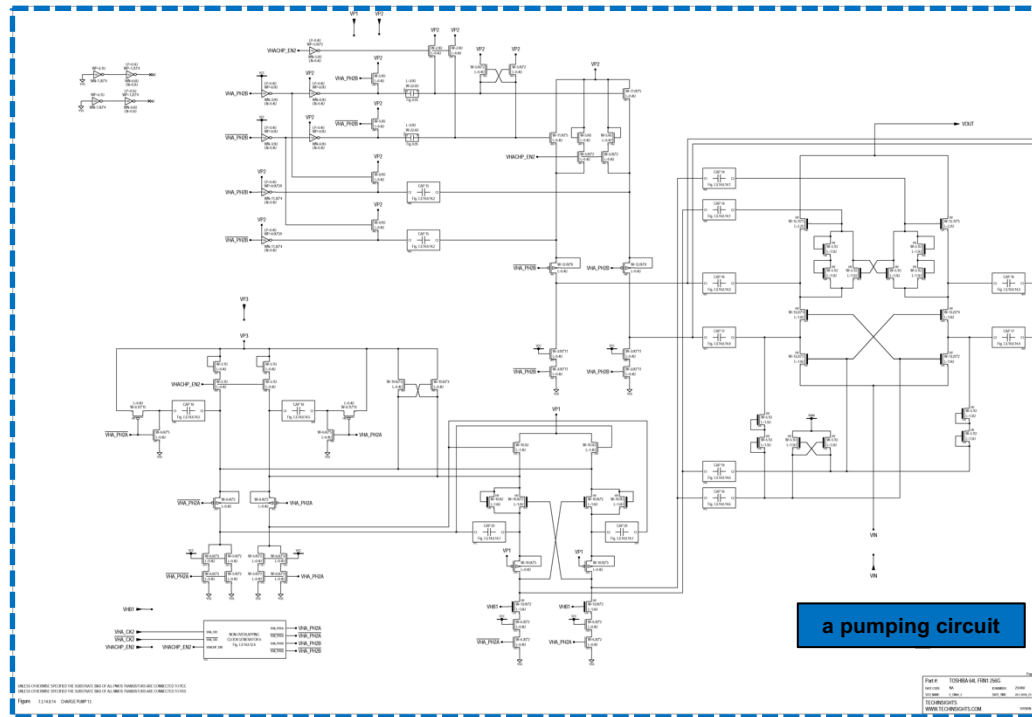
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Product
	<p data-bbox="636 267 966 329">operable to receive a supply voltage (VCC)</p>  <p data-bbox="636 792 1827 865">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

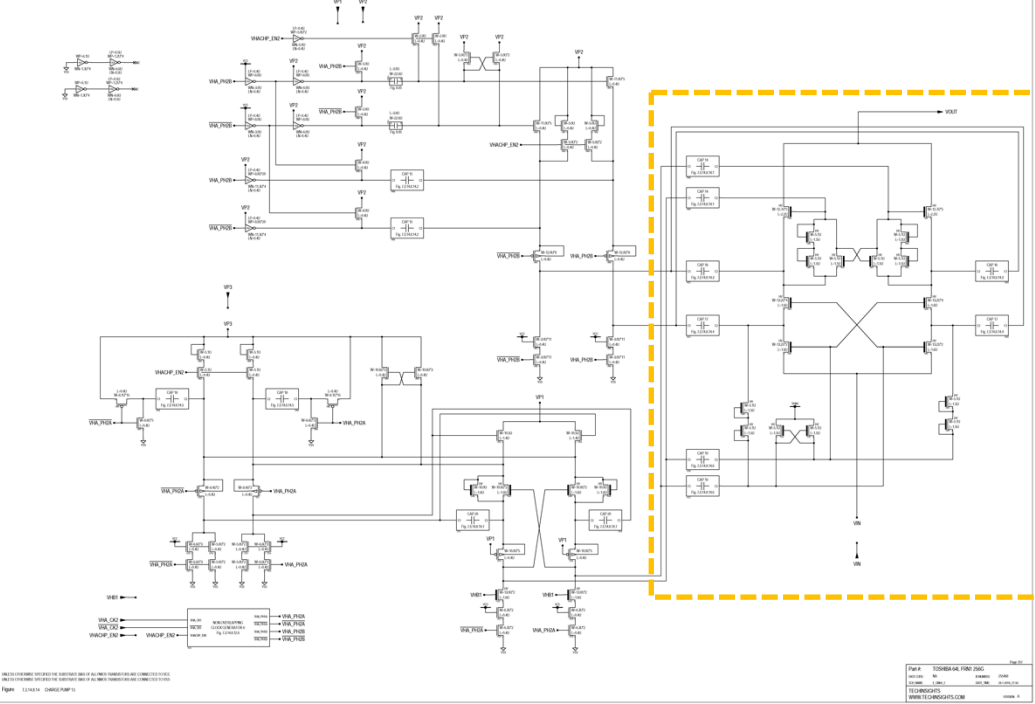
Claim 1	Accused Product
	 <p>The diagram shows three charge pumps, labeled CHARGE PUMP 12, CHARGE PUMP 13, and CHARGE PUMP 14, each enclosed in a dashed yellow box. Each pump has three input pins (VP1, VP2, VP3) and one output pin (VOUT). A callout box labeled 'comprising one or more stages' points to the input pins of the first pump. A callout box labeled 'a pumping circuit' points to the internal circuitry of the first pump. The first pump (CHARGE PUMP 12, Fig. 7.3.14.8.12) has inputs VHA_CK3, VHA_CK3, and VHACHP_EN3. The second pump (CHARGE PUMP 13, Fig. 7.3.14.8.14) has inputs VHA_CK2, VHA_CK2, and VHACHP_EN2. The third pump (CHARGE PUMP 14, Fig. 7.3.14.8.17) has inputs VHA_CK1, VHA_CK1, and VHACHP_EN1. Each pump also has a VHB1 input and a VBI output.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

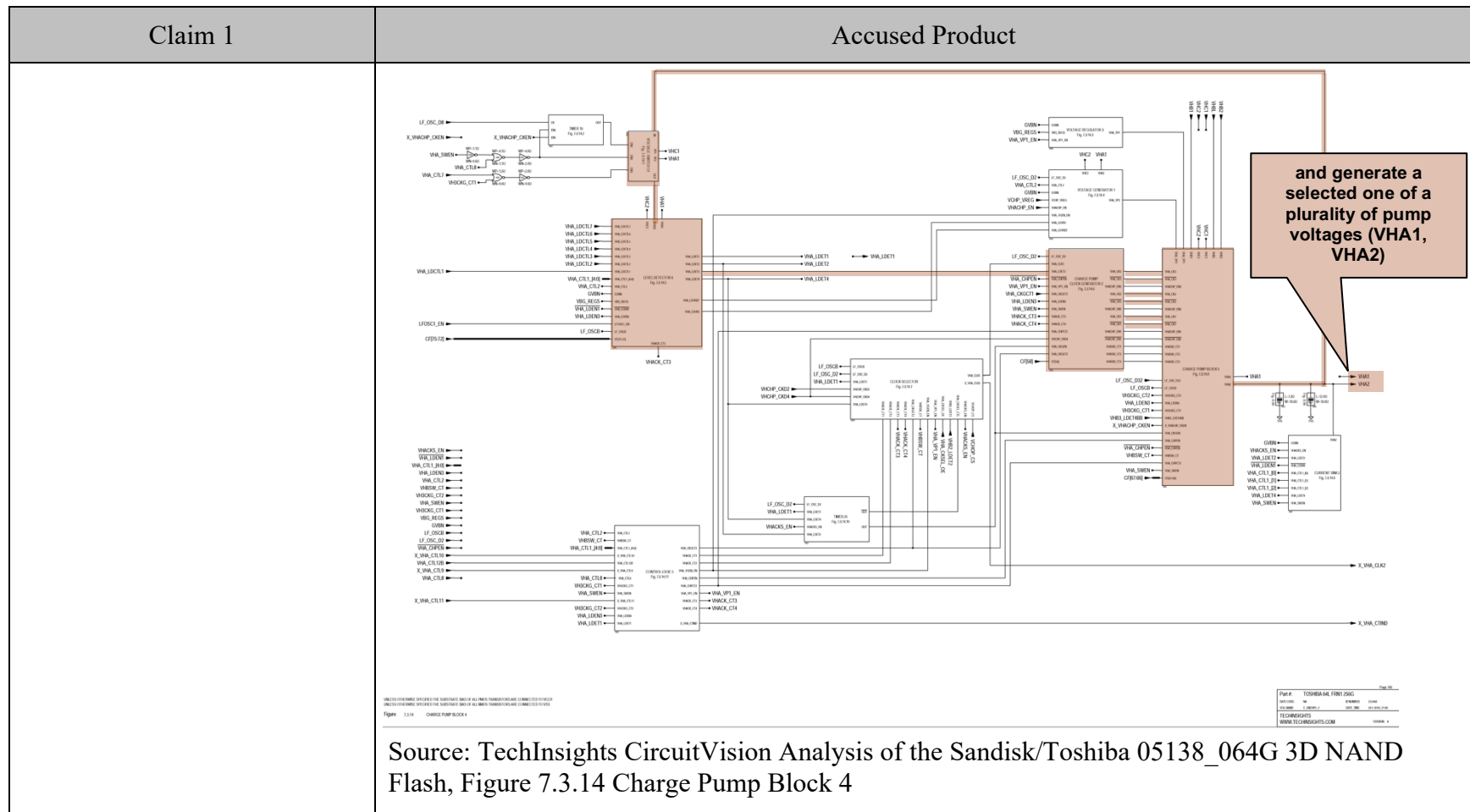
Claim 1

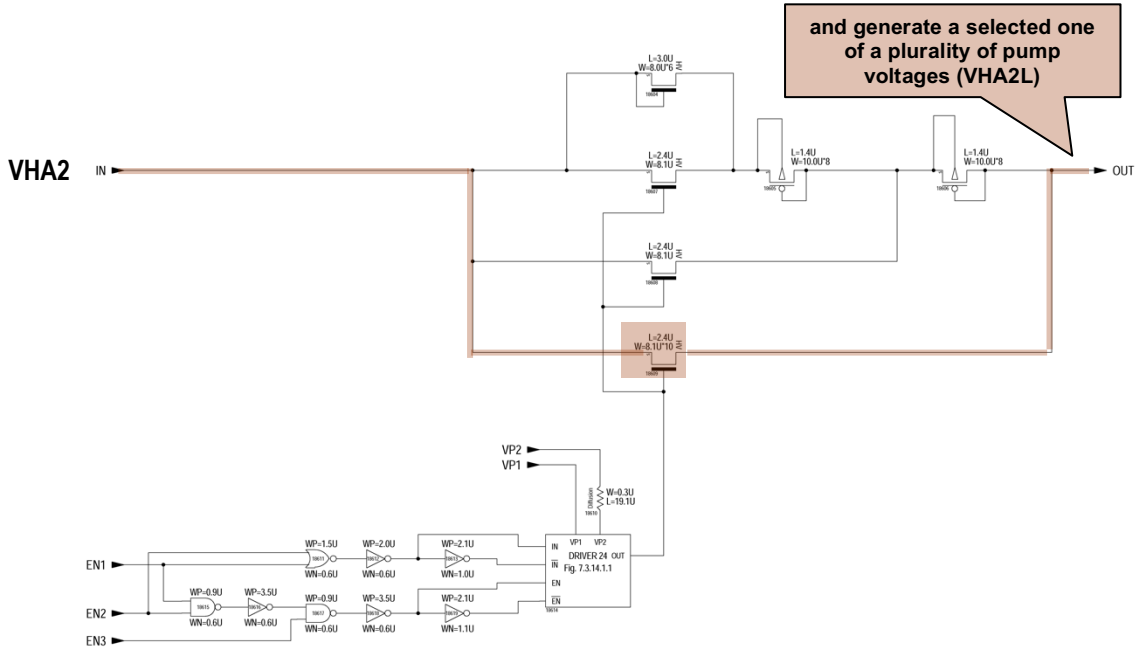
Accused Product

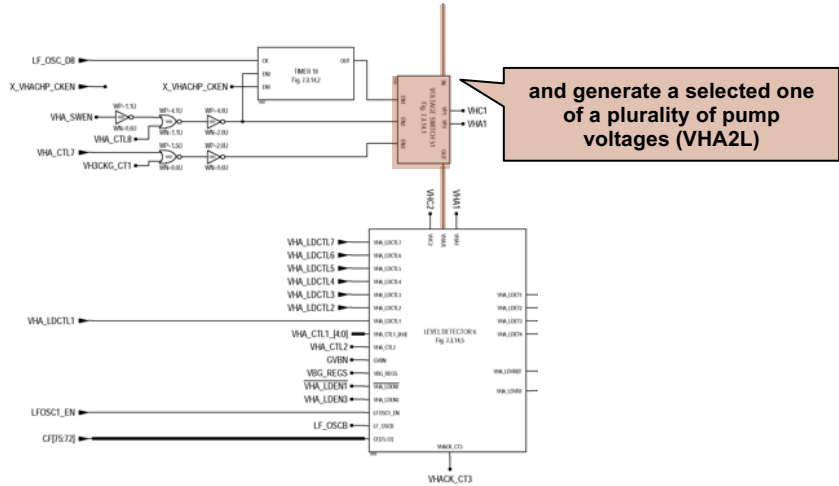


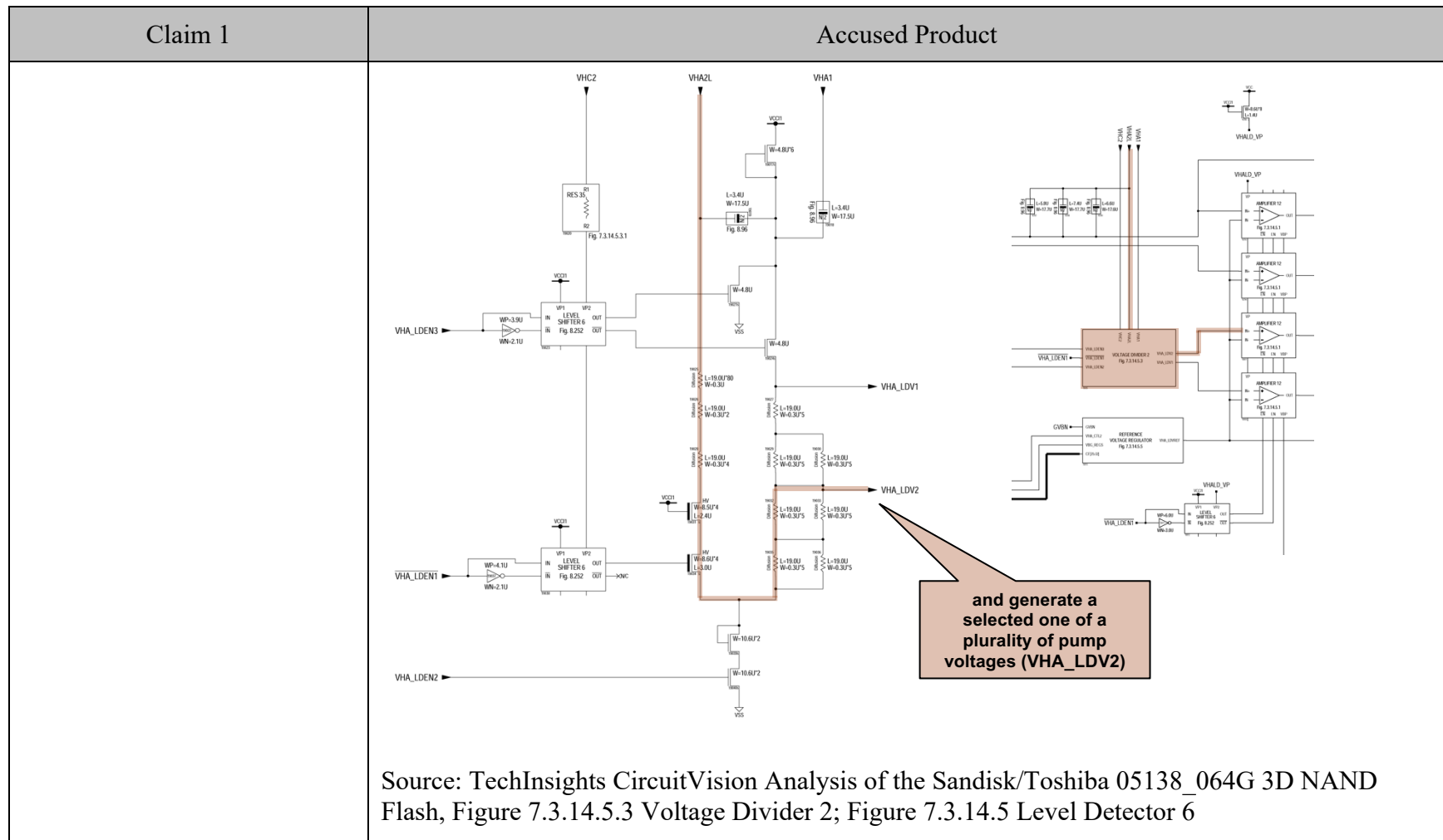
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>



Claim 1	Accused Product
	 <p>The diagram shows a circuit for a voltage switch (VHA2). It features an input (IN) and an output (OUT). The circuit includes several transistors and capacitors. A callout box points to a specific transistor and capacitor combination, stating: "and generate a selected one of a plurality of pump voltages (VHA2L)".</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>



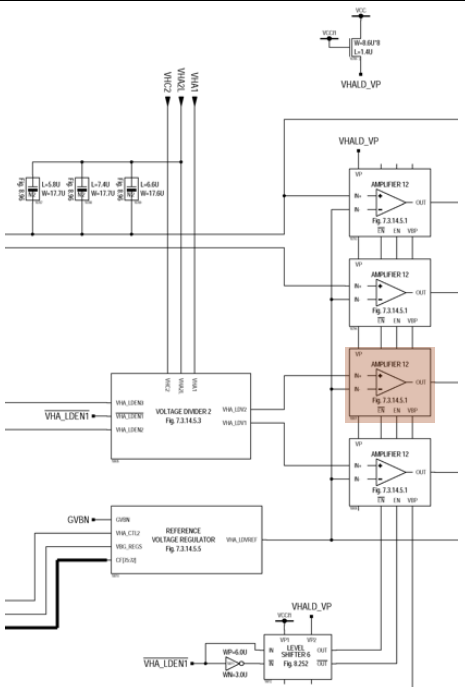
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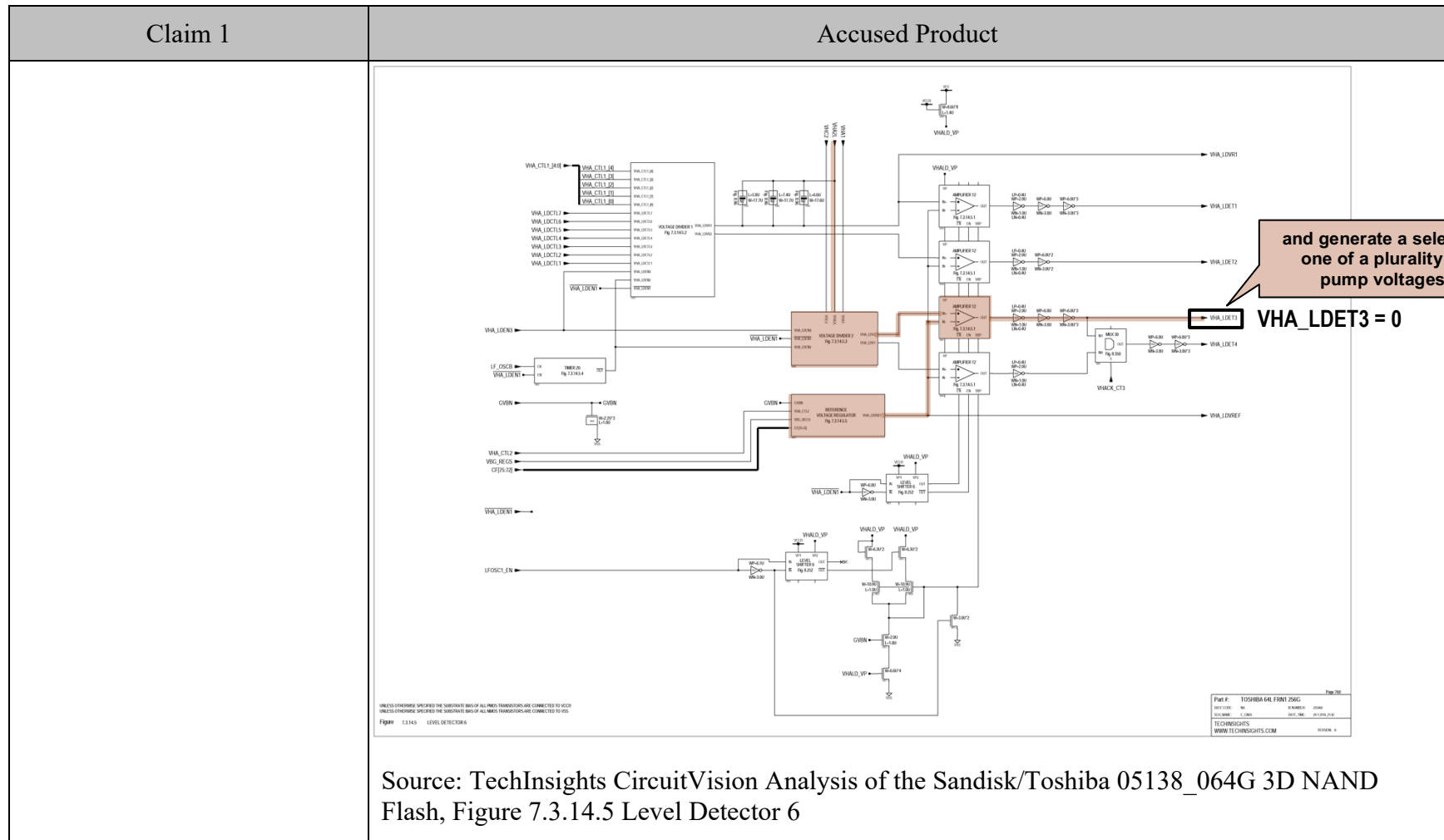
Claim 1

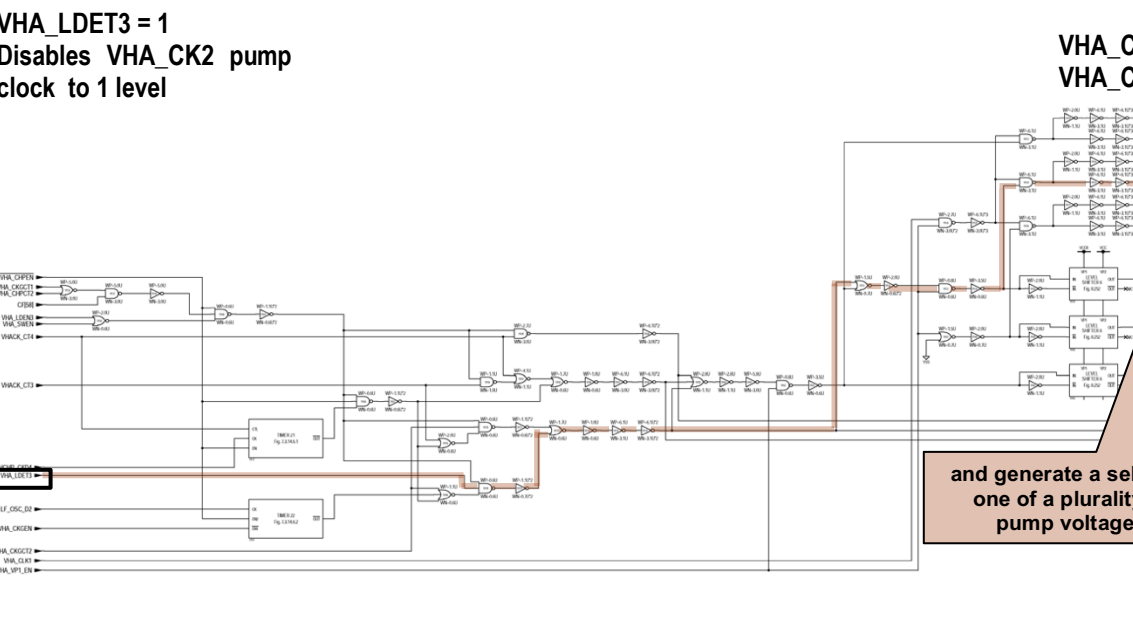
Accused Product

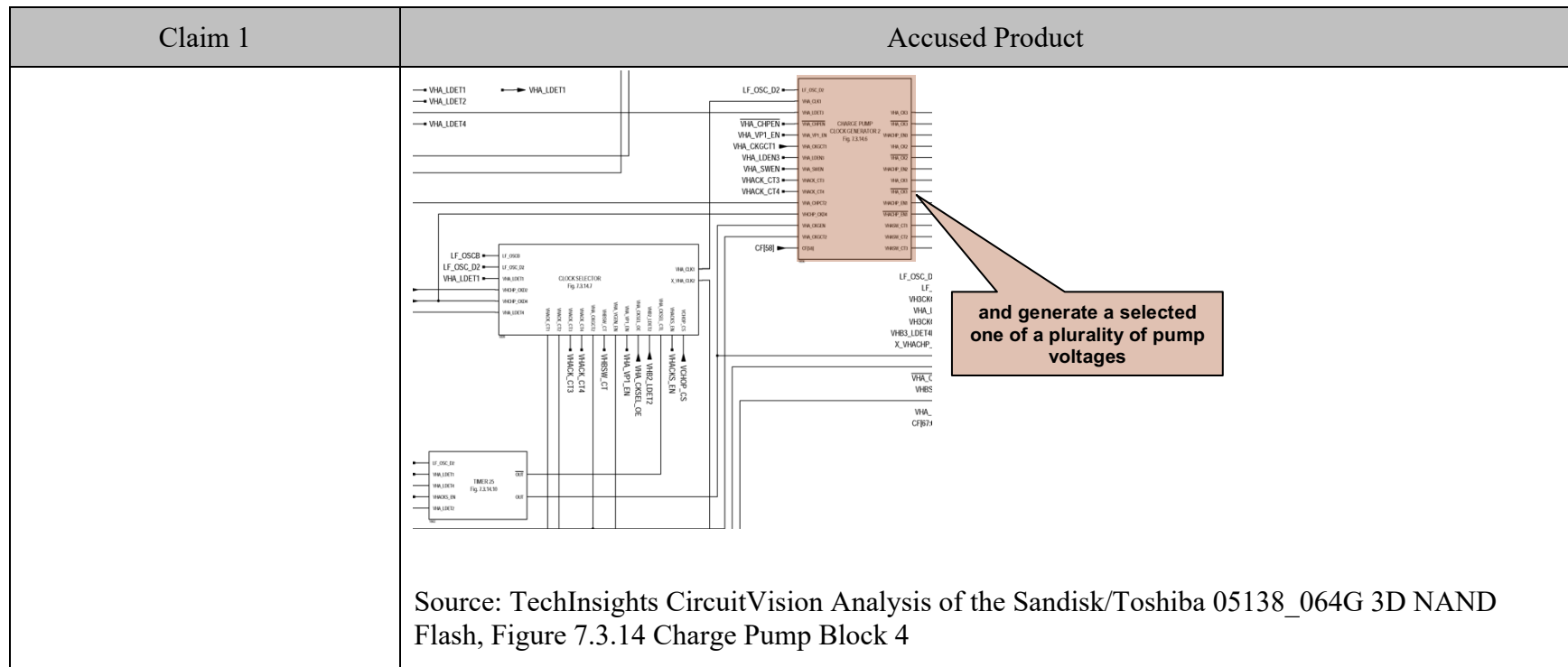
The diagram illustrates a Reference Voltage Regulator circuit. It features a multi-stage differential amplifier with input nodes labeled VBIAS, VBIAS, and VBIAS. The output of the amplifier is connected to a current mirror array, which is used to generate a selected one of a plurality of pump voltages (VHA_LDVPREF). The circuit includes various transistors with dimensions (W, L) and a current source (I_{REF}). A feedback loop is shown with a resistor (R_{FB}) and a capacitor (C_{FB}). The output of the feedback loop is connected to the input of the amplifier. The circuit is powered by GND and VDD. A note indicates that the substrate bias of all NMOS transistors is connected to GND.

Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

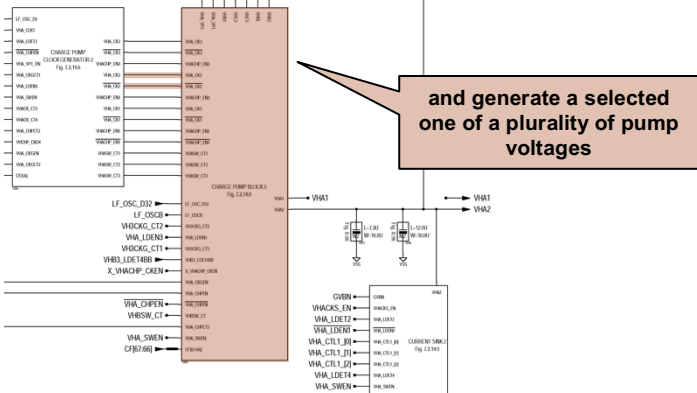
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

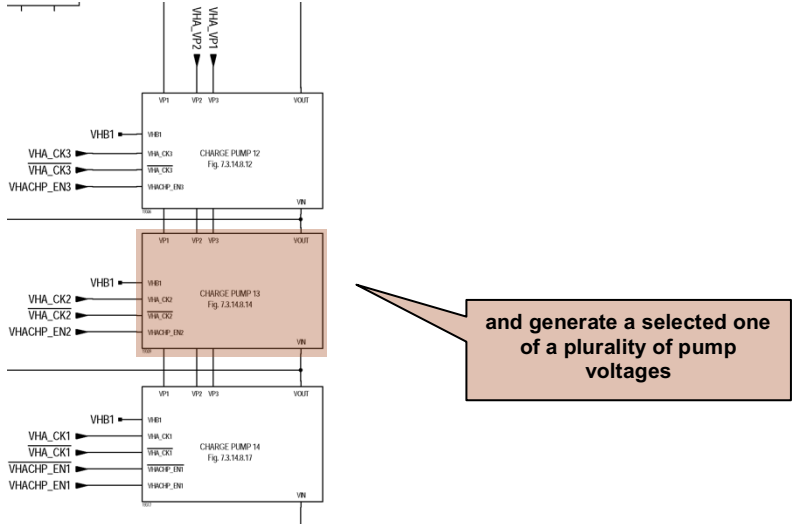


Claim 1	Accused Product
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p>  <p>VHA_CK2 = 1 VHA_CK2* = 0</p> <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>



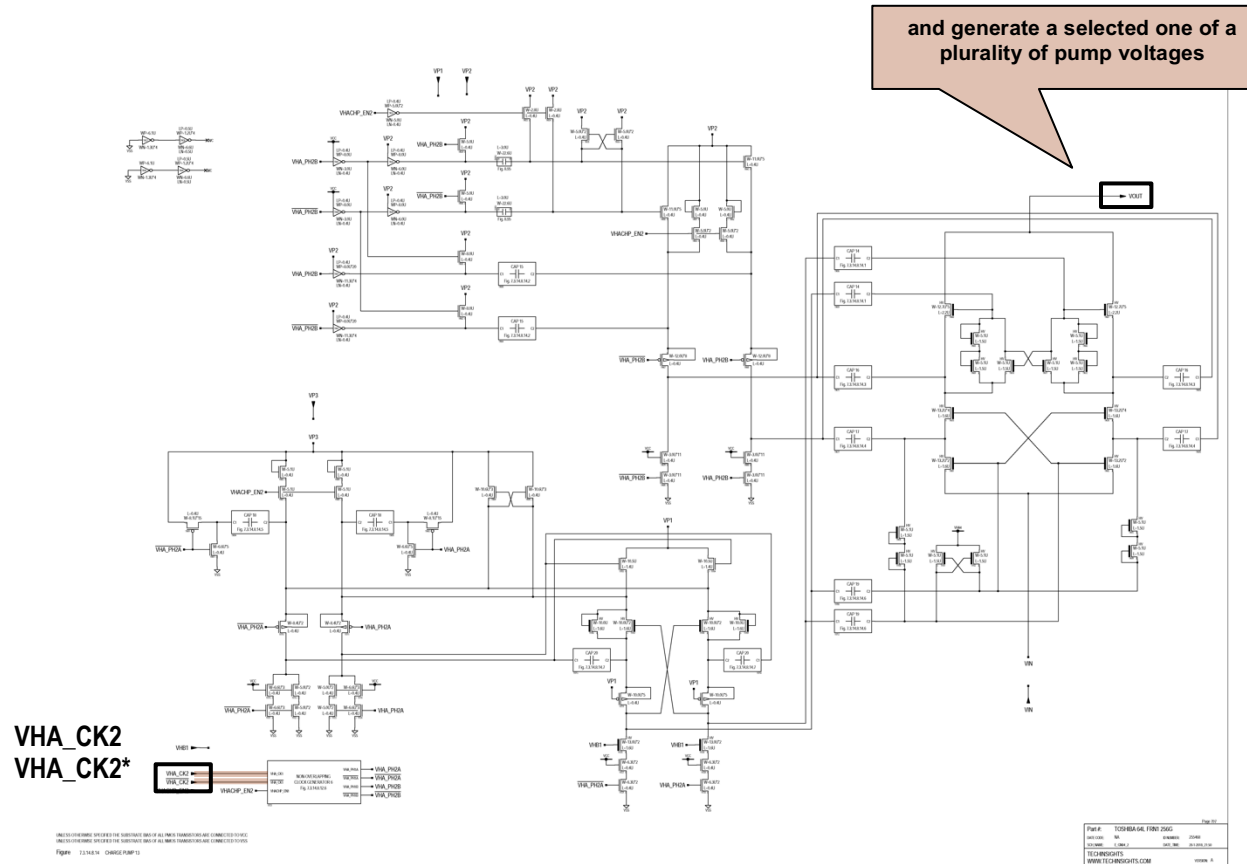
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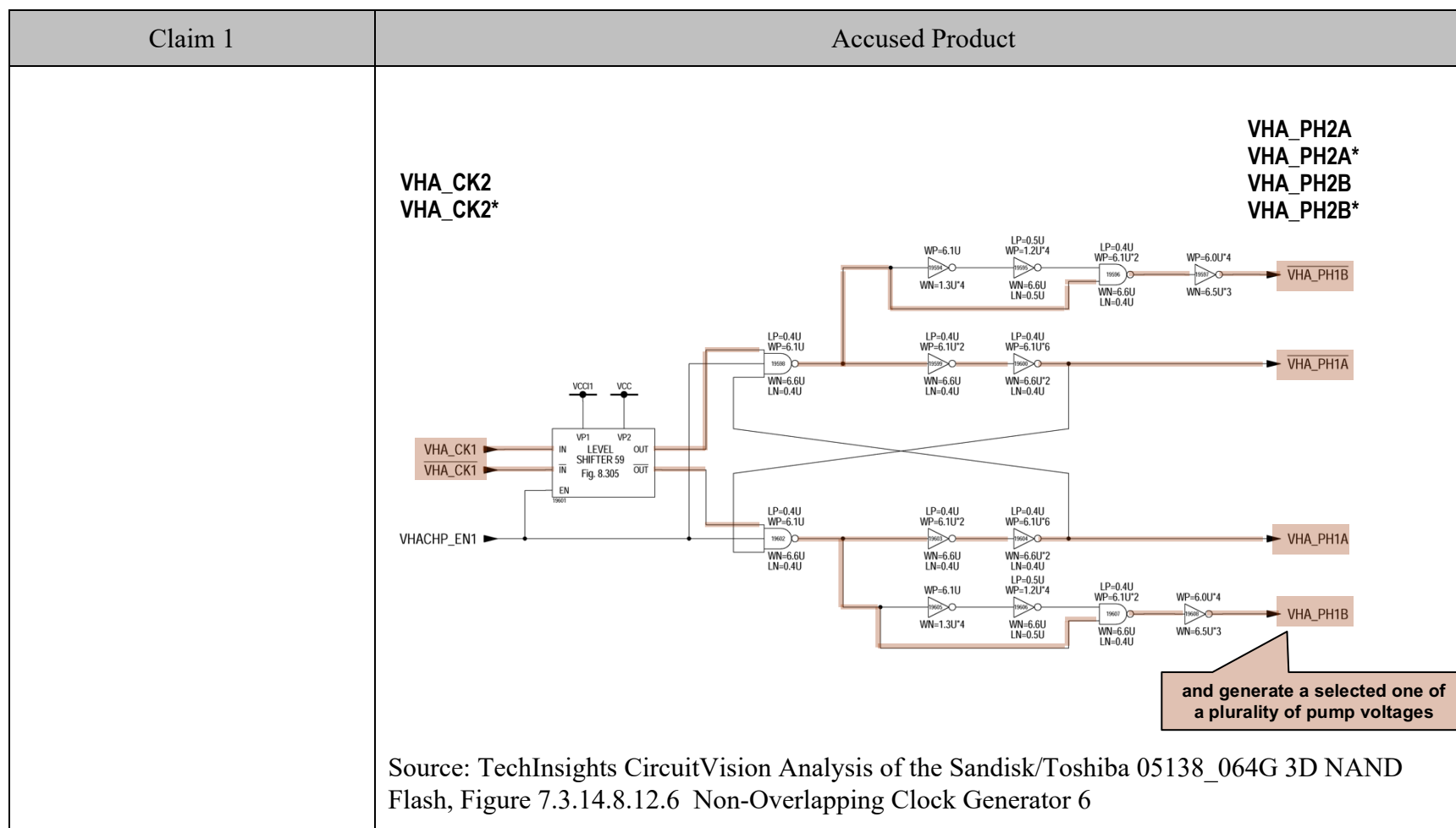
Claim 1	Accused Product
	 <p data-bbox="1029 332 1323 430">and generate a selected one of a plurality of pump voltages</p> <p data-bbox="630 698 1827 771">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

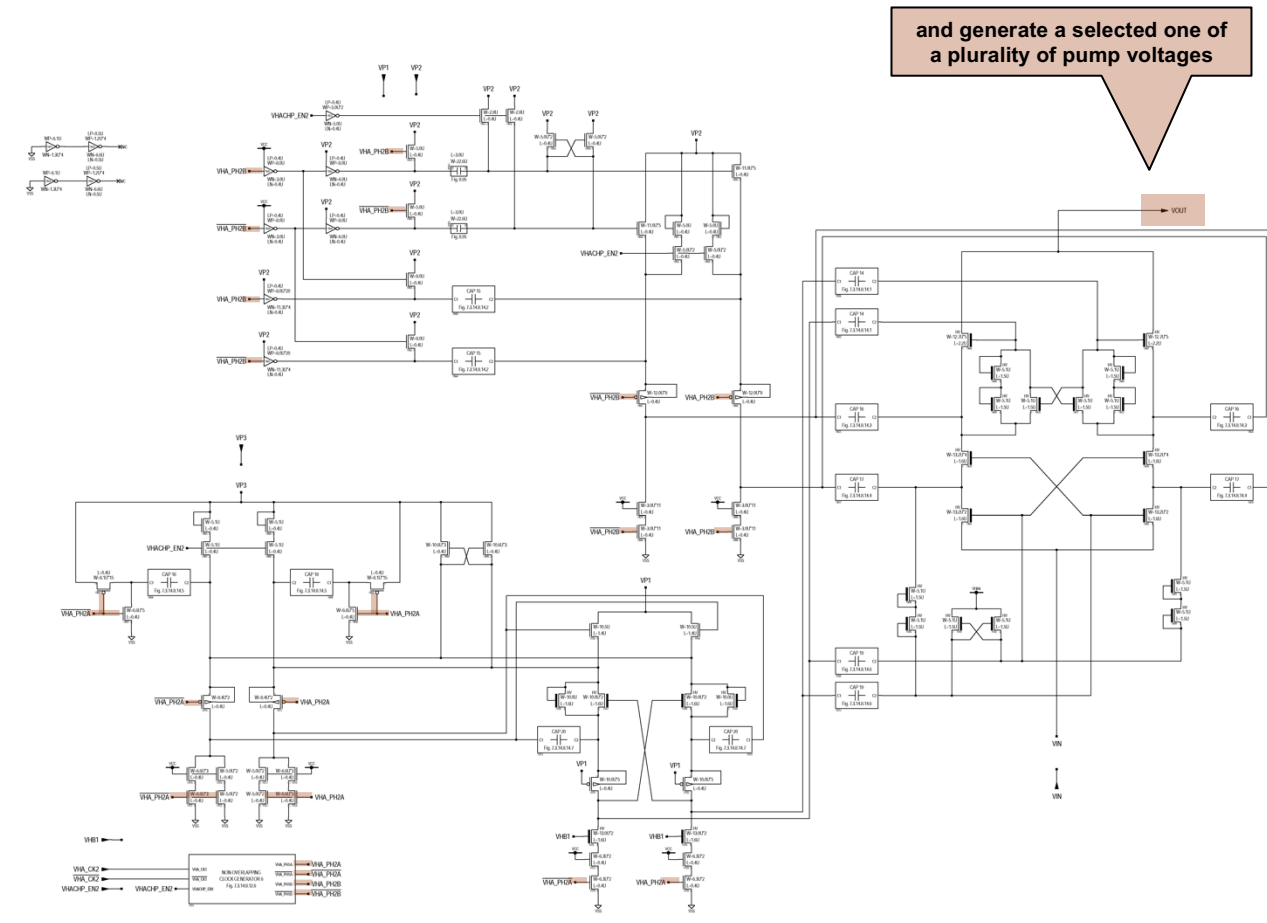
Claim 1	Accused Product
	 <p>The diagram shows three charge pump blocks stacked vertically. Each block has inputs for VHB1, VHA_CK, VHA_CK2, VHA_CK3, and VHACHP_EN. The top block is labeled 'CHARGE PUMP 12 Fig. 7.3.14.8.12', the middle block is 'CHARGE PUMP 13 Fig. 7.3.14.8.14', and the bottom block is 'CHARGE PUMP 14 Fig. 7.3.14.8.17'. A callout box points to the middle block with the text: 'and generate a selected one of a plurality of pump voltages'.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block</p>

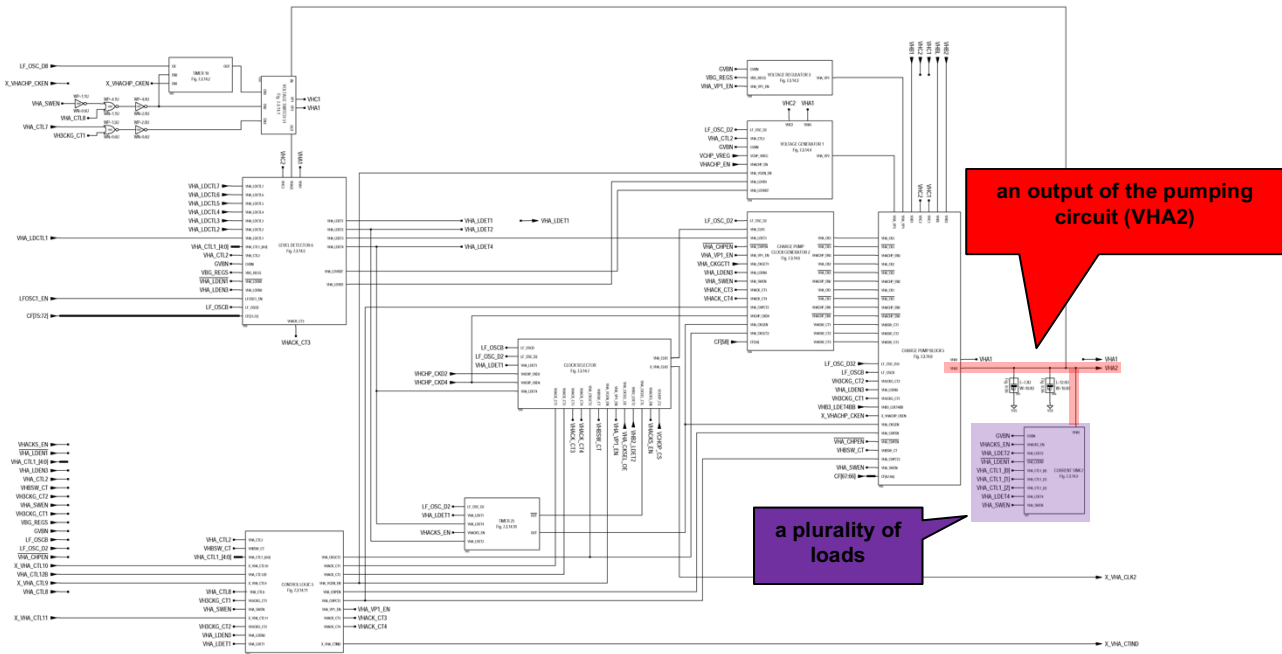
Claim 1

Accused Product



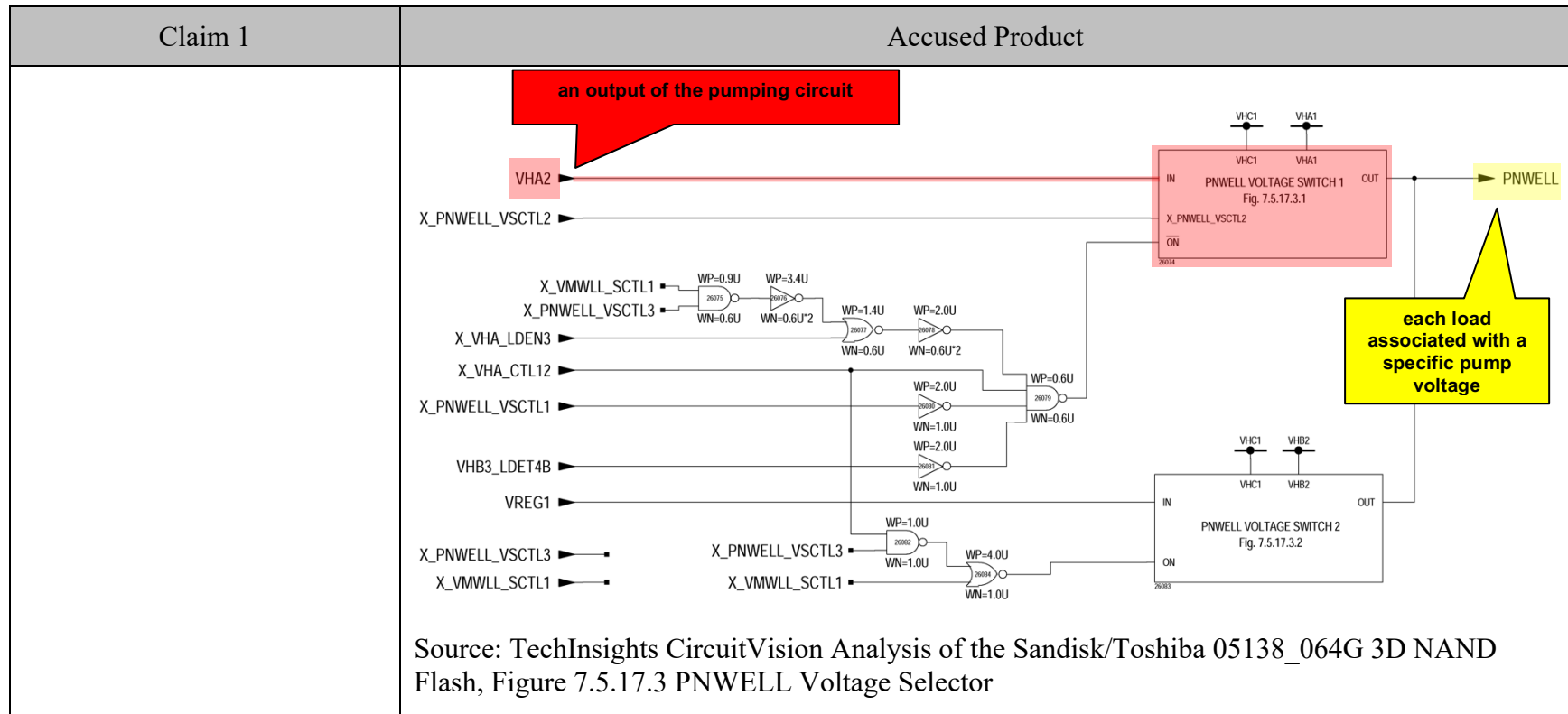


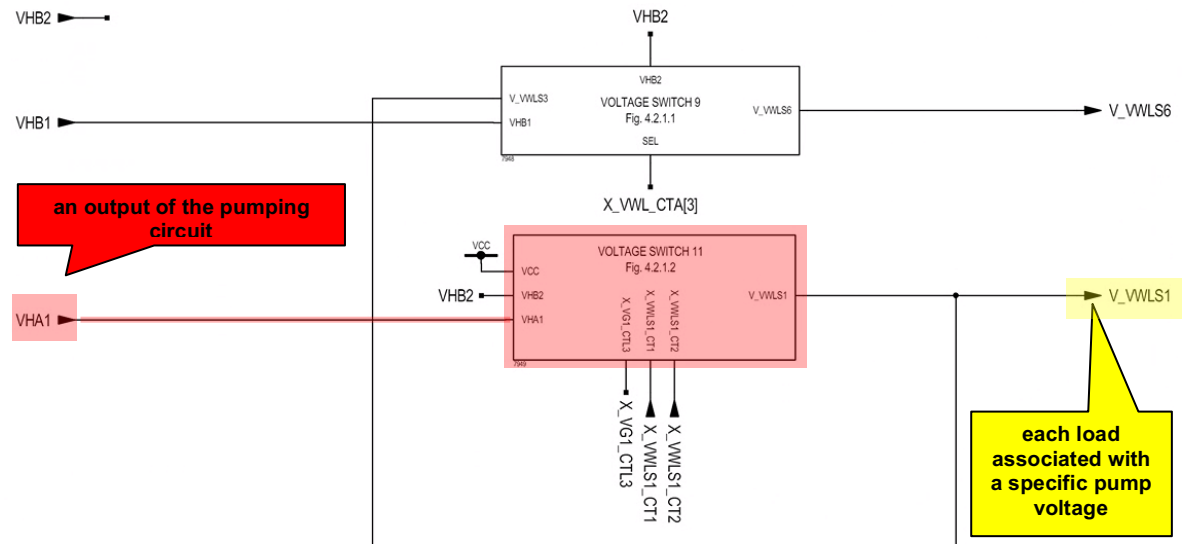
Claim 1	Accused Product
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>
1[b] a plurality of loads selectively coupleable to an output of the pumping circuit,	Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.

Claim 1	Accused Product
<p>each load associated with a specific pump voltage; and</p>	<p>For example, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p><i>See, e.g.:</i></p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

[illegible]

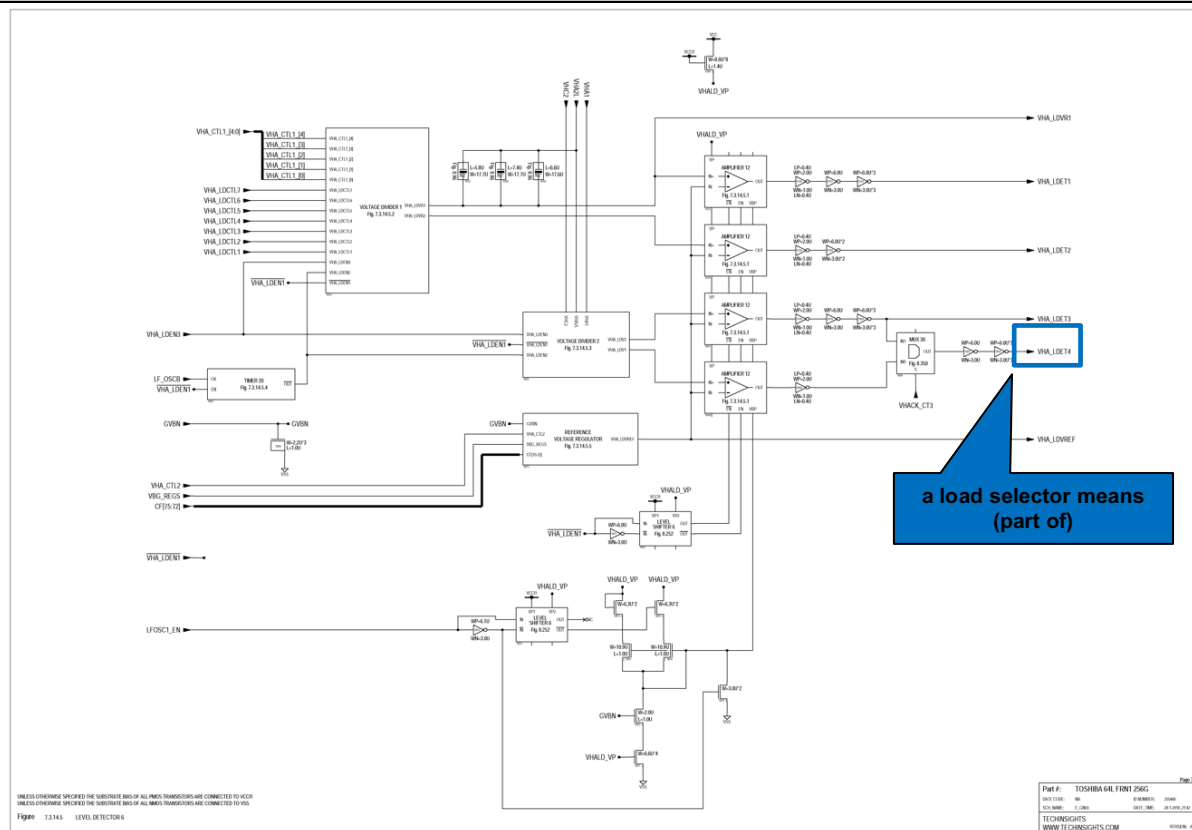
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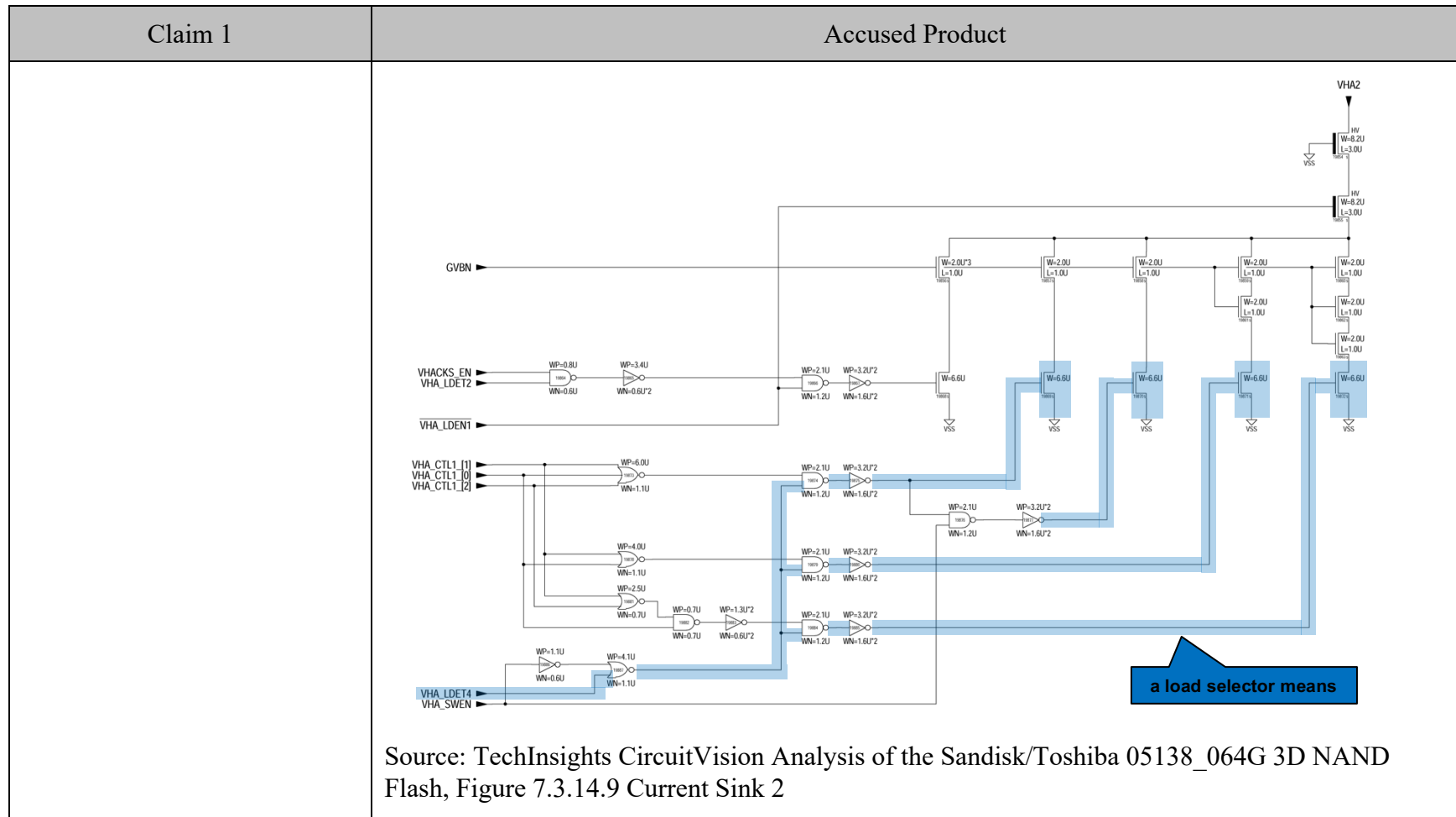
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>1[c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

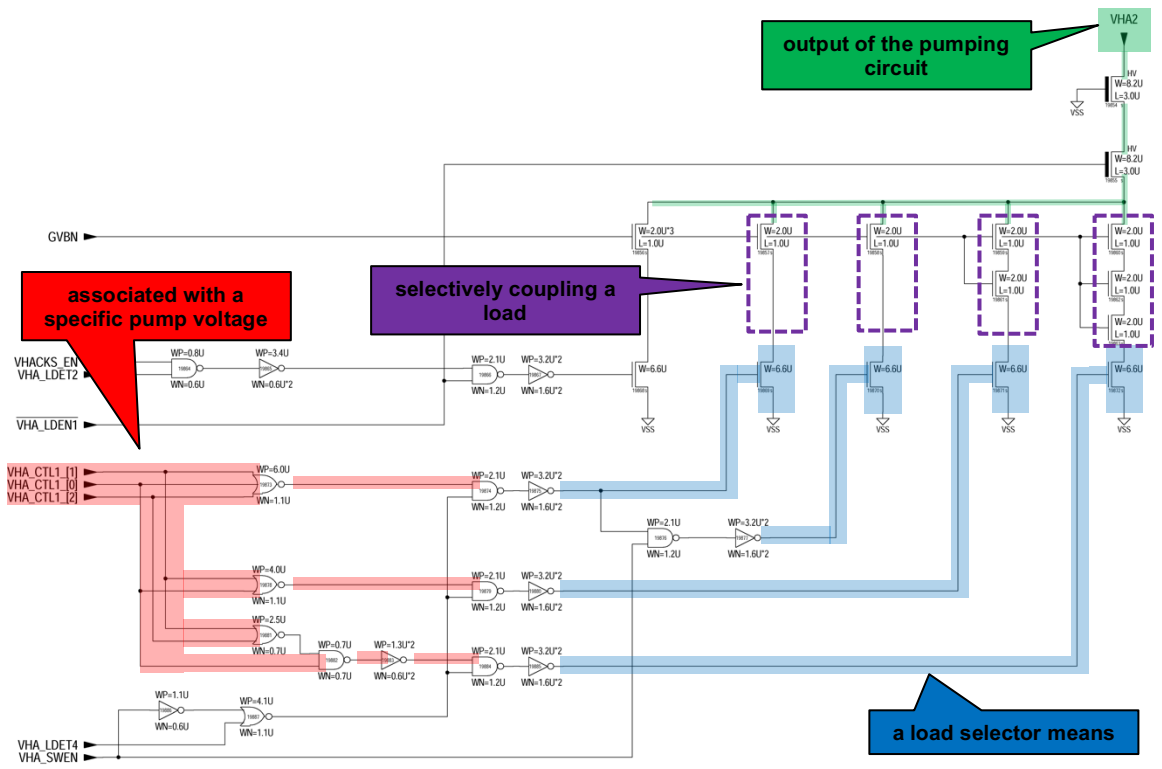
Claim 1

Accused Product



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6



Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

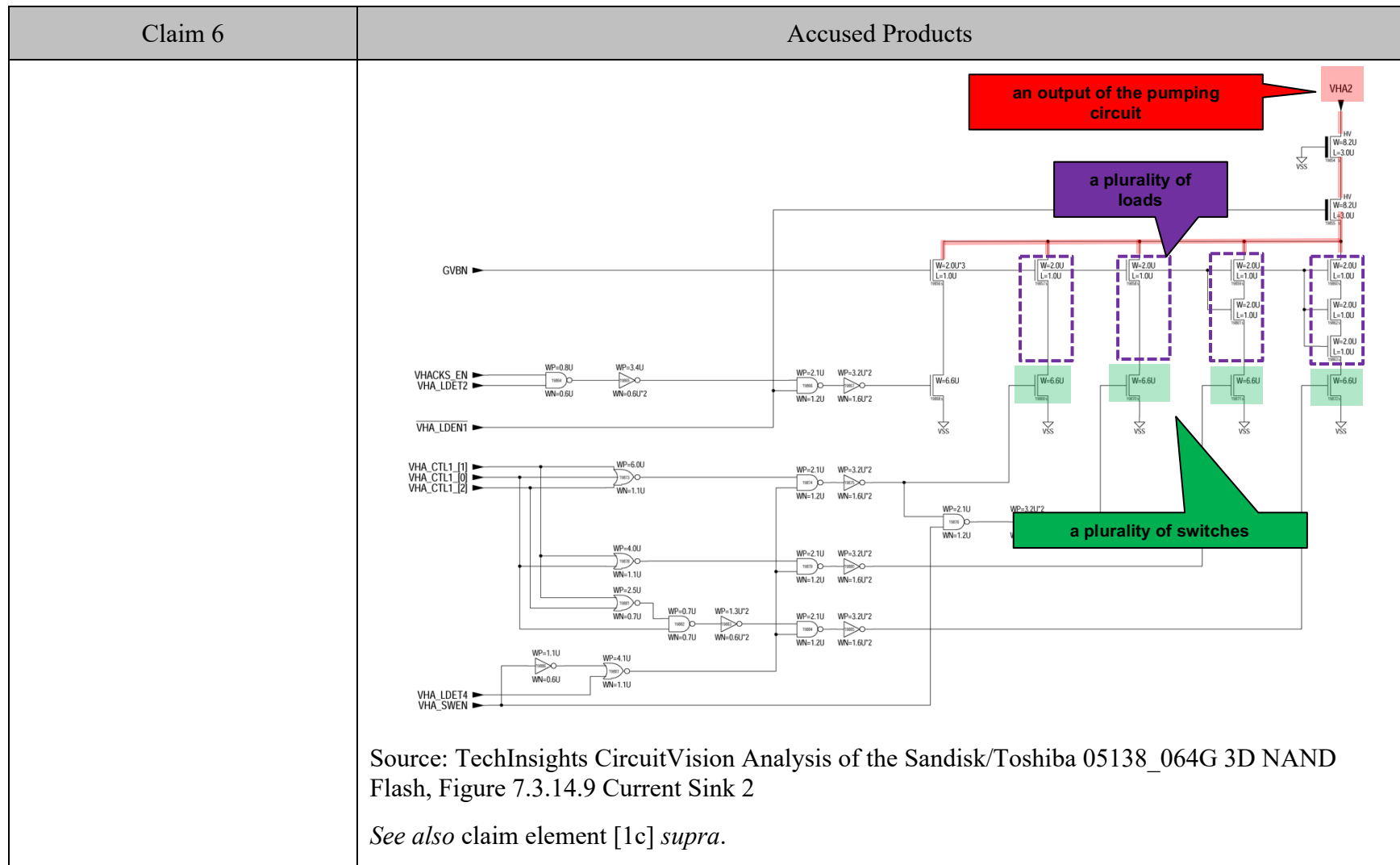
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (V_{ref}).	

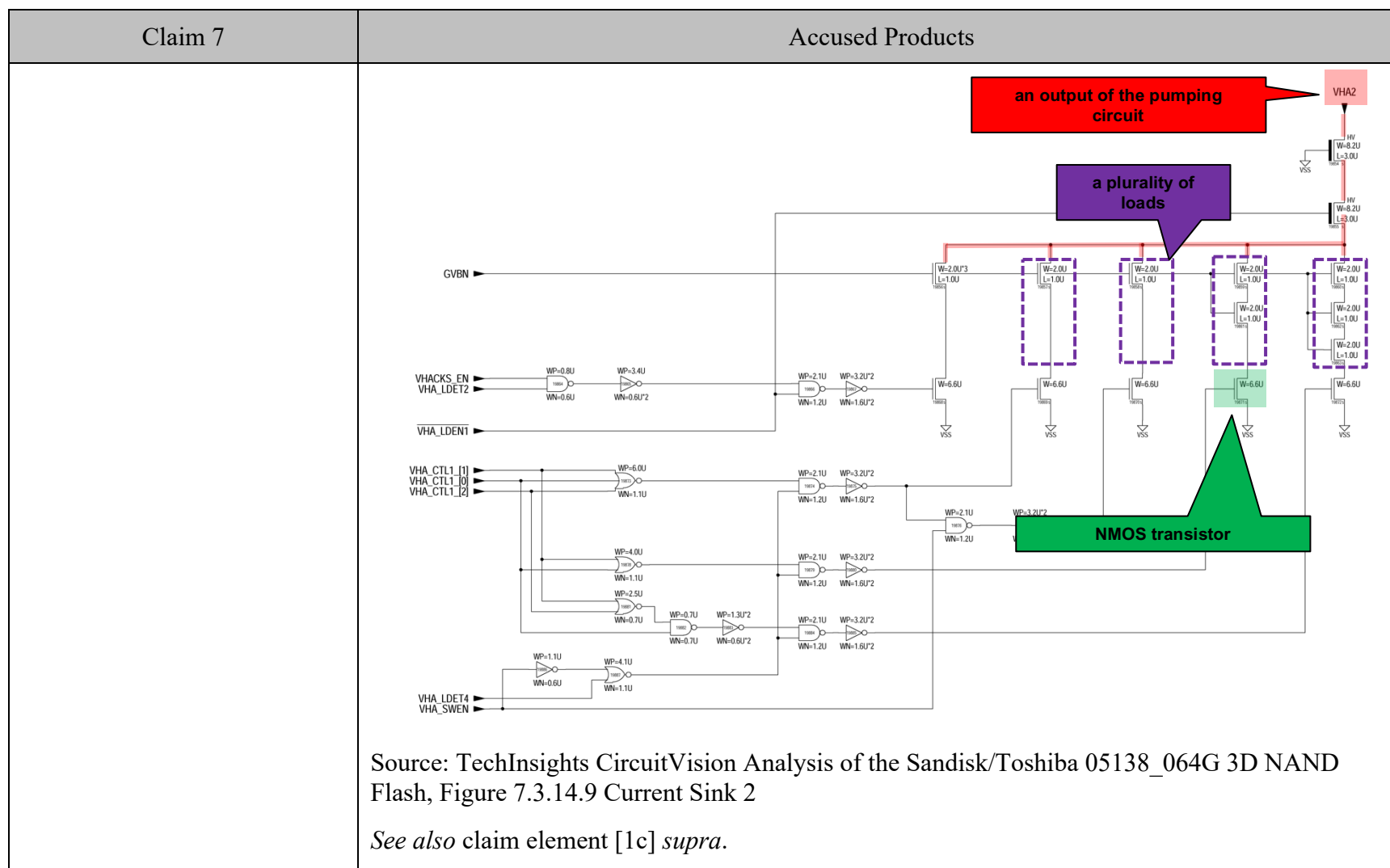
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>



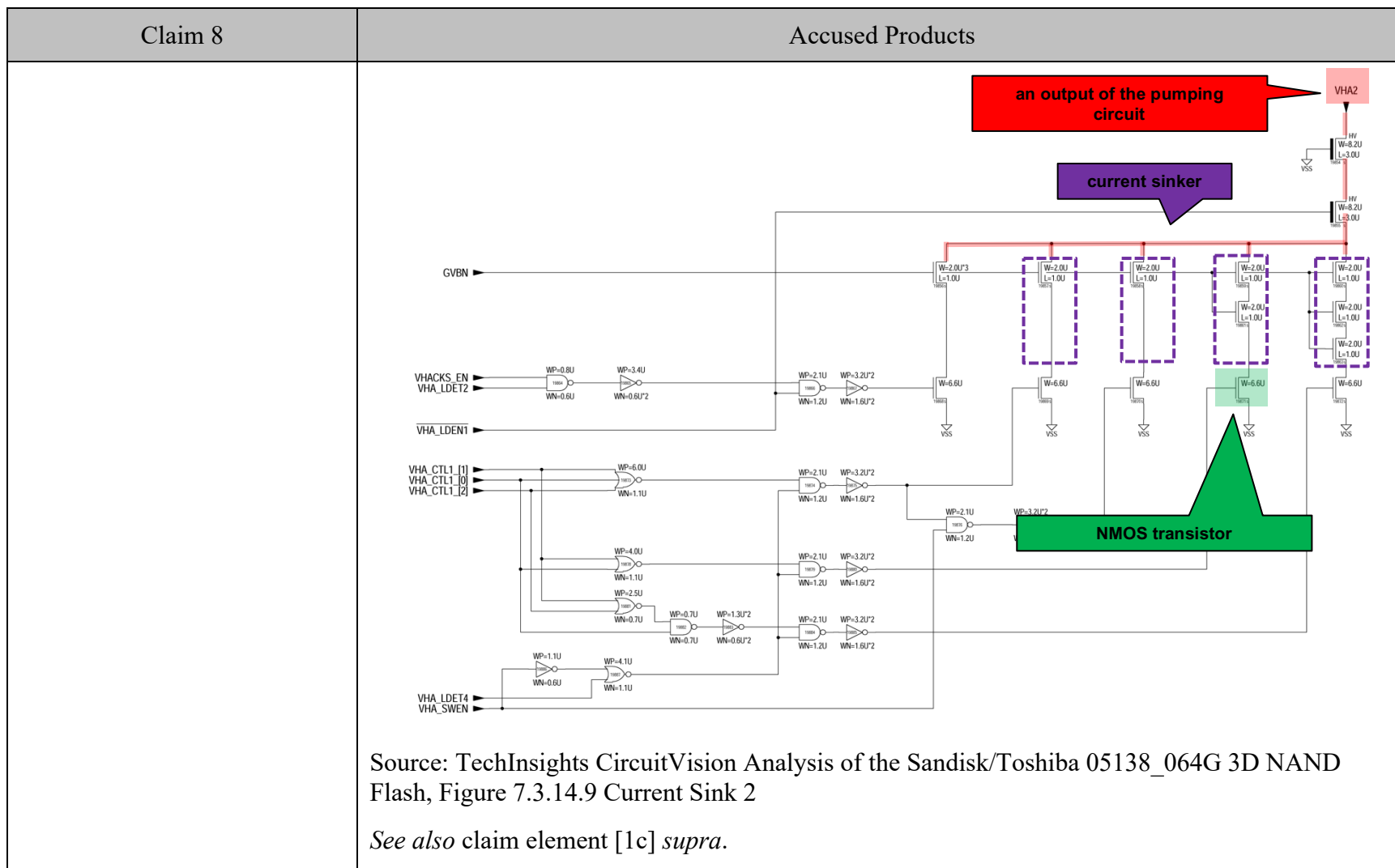
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



Claim 8

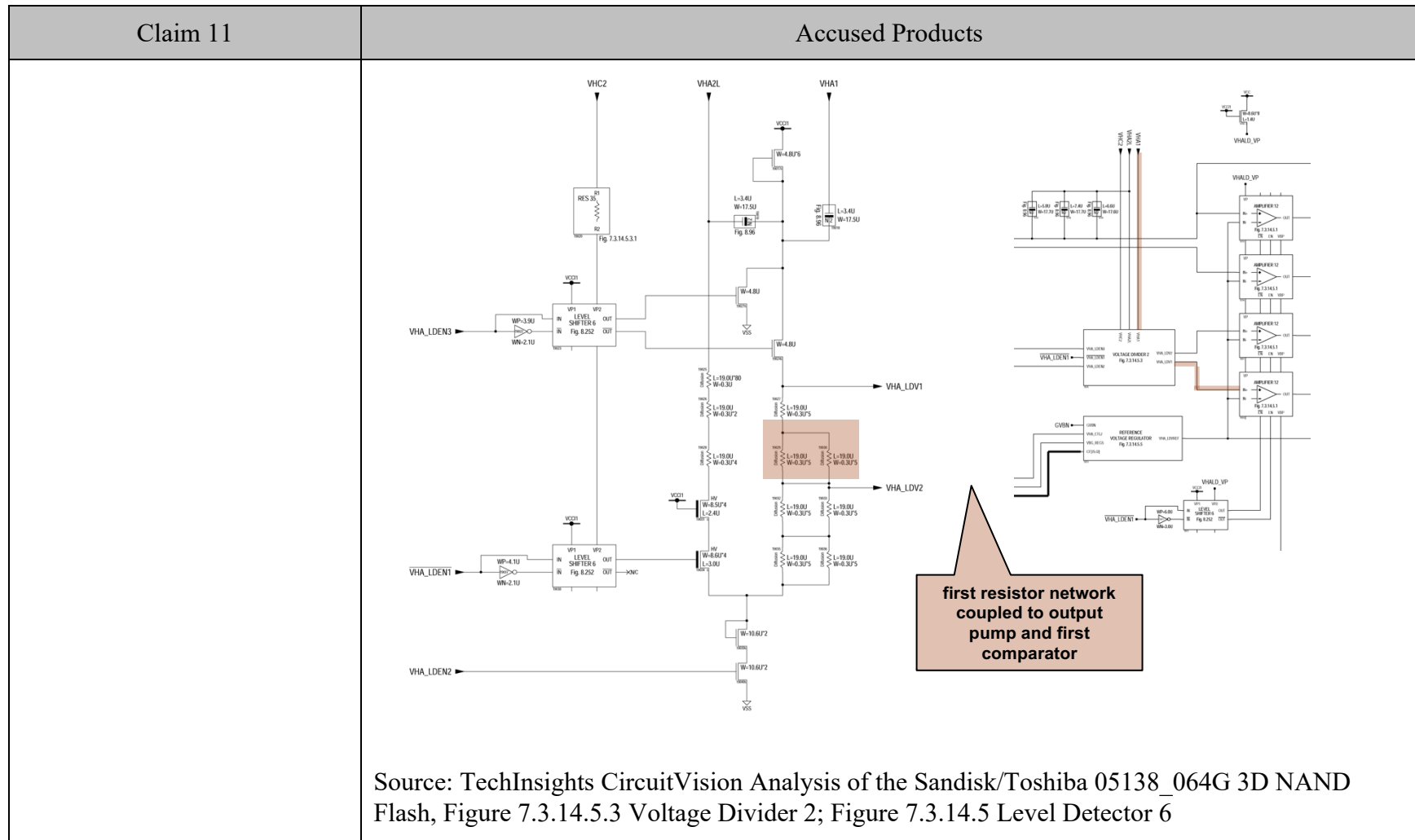
Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

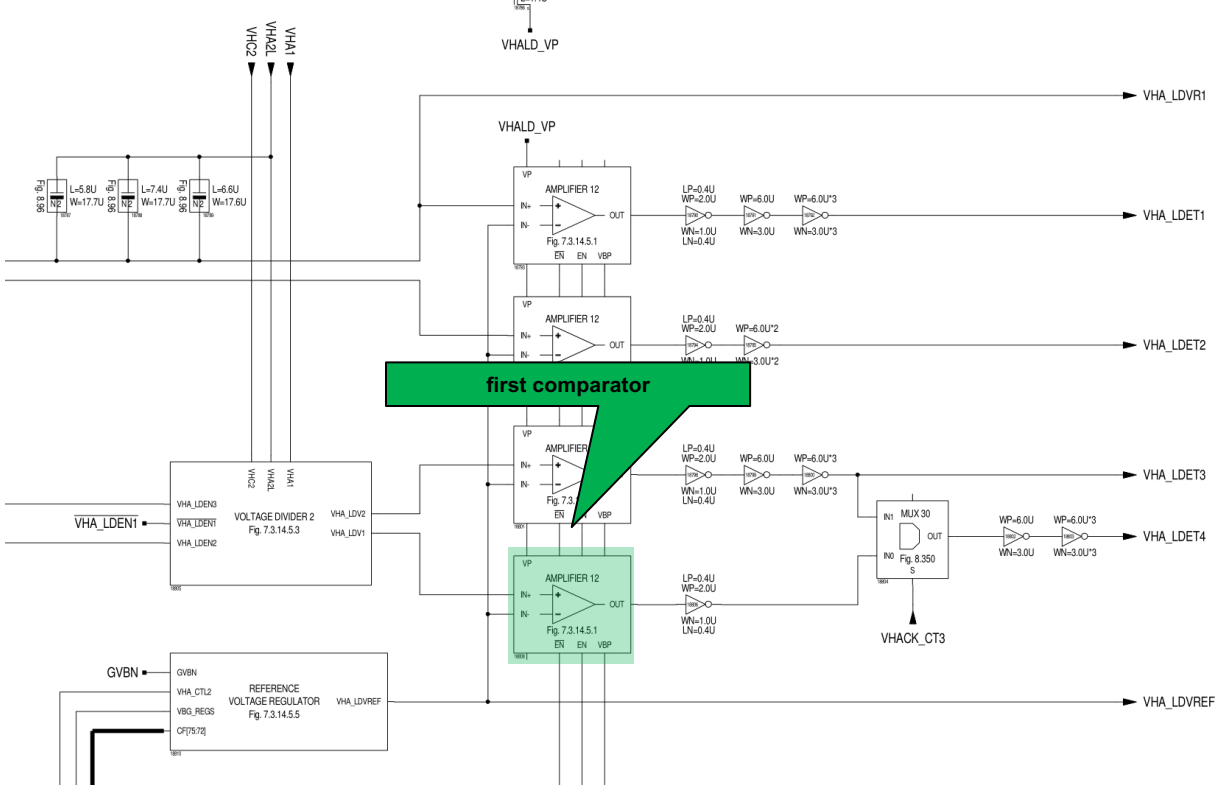


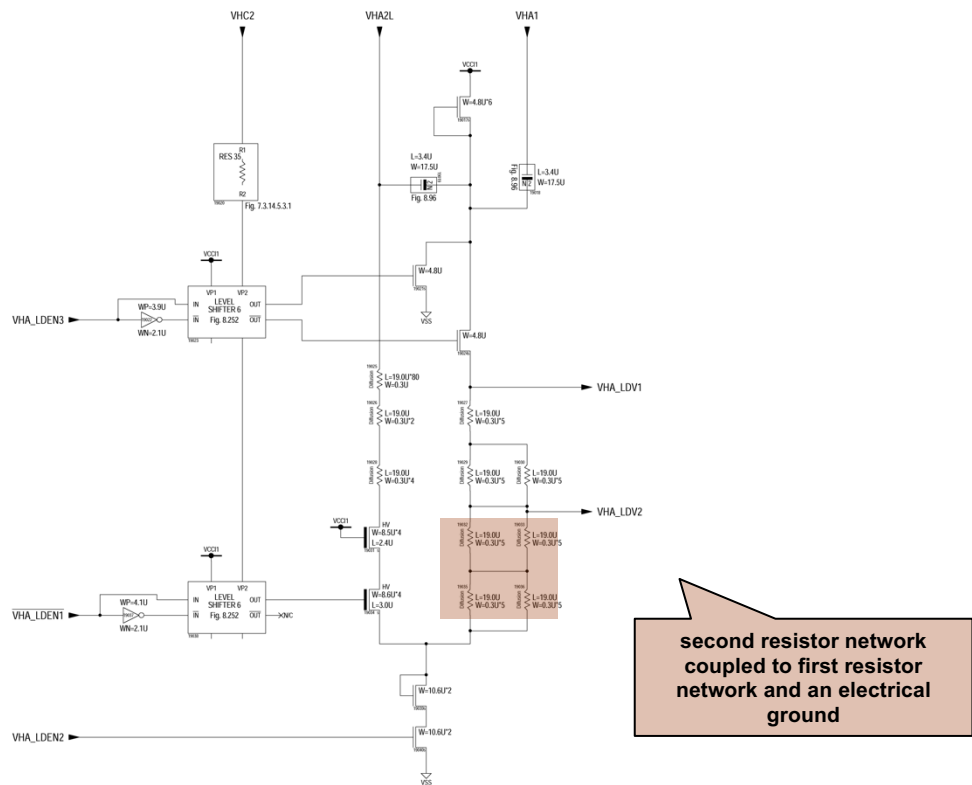
Claim 11

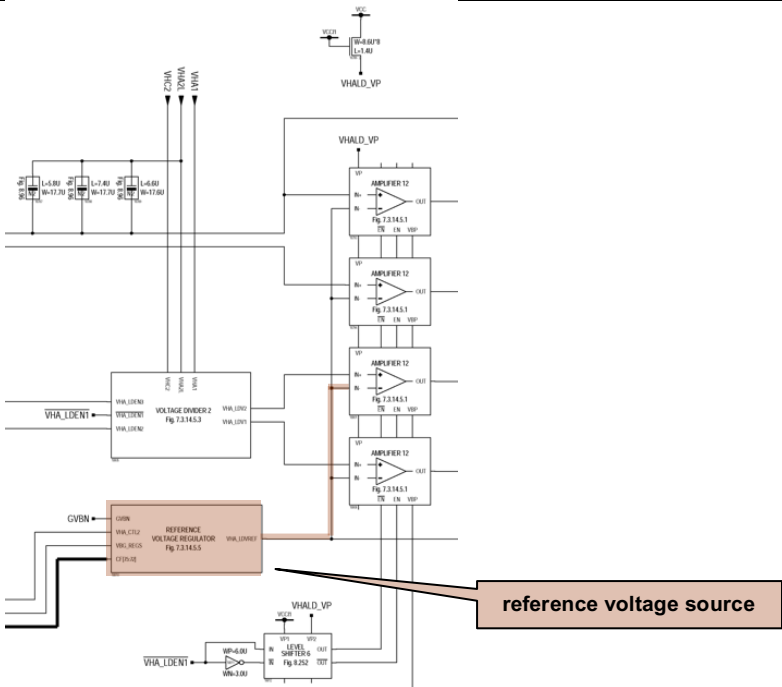
Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>



Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
coupled to an electrical ground; and	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>